Analog and Digital Fractional-n PLL Frequency Synthesis: A Survey and Update

By Bar-Giora Goldberg
Sciteq/Osicom

The Phase Lock Loop (PLL) has become a fundamental part of radio technology and is clearly the method of choice for generating signals in radio and timing applications. The past few years have seen the advance of fractional-n, a PLL technology that allows improved phase noise and switching speed. Traditionally, fractional-n uses analog compensation mechanisms to suppress spurious signals. This technology has not yet matured, and while division ratios have been reduced, other system parameters have deteriorated, resulting in equivalent performance rather than the advantages we expect over integer-n PLL chips. This will be corrected in due time.

There is also emerging activity in the application of complex DSP operations for all-digital fractional-n implementation involving oversampling, noise shaping and Sigma-Delta modulation. There are no such devices in the market yet, but we expect to see them emerging in 1999.

The purpose of this article is to briefly survey fractional-n principles, demonstrate various methods and compare their potential and actual performance levels.

Introduction to the PLL
The PLL technique is a simple negative feedback mechanism with a divider in the feedback. This structure is very economical for multiplying crystal reference, $F_r$, many times (thousands), while maintaining good control of the output signal ($F_0 = NF_r$, $N$ an integer) spectral noise profile. See Figure 1 for the basic PLL architecture.

All PLL designs for frequency synthesis use the 2nd order model. The main block models in the Laplace domain are:

- **VCO** as $Kv/s$ (the VCO is an integrator),
- **phase (or phase-frequency) detector (PFD)** as $K_d$ (V/rad or A/rad)
- and the **loop filter** as $F(s) = (1+sT^2)/sT$.

Close to the carrier (<100 Hz in cellular applications), the output noise profile is determined mainly by the reference crystal noise, then by the phase detector noise up to the loop bandwidth, and then by the VCO. A typical composite phase noise from these 3 sources is shown in Figure 2.

The crystal and PFD noises are corrupted by $20\log(N)$ within the loop bandwidth but filtered by the loop transfer function

$$H(s) = N(2\xi\omega_n + \omega_n^2)/(s^2 + 2s\xi\omega_n + \omega_n^2)$$
at frequency offsets beyond the loop bandwidth (usually given by the frequency in which the open loop gain is 1, or approximately \( \omega_n/2 \pi \)).

The VCO noise, on the other hand, is multiplied by \( s^2/(s^2 + 2s\xi\omega_n + \omega_n^2) \). Thus its noise is heavily attenuated close to the carrier; but thereafter, at frequencies above the loop filter, VCO noise passes without attenuation. 3rd and 4th order loops are a modification of the 2nd order to further attenuate reference spurious and noise.

Inside the loop bandwidth, however, the crystal and PFD noise amplification by 20log(\( N \)) dB, is a very significant number. In the US and the Far East, \( N \gg 30000 \), or approximately 90 dB noise corruption. In Europe and other countries using GSM in the 1.8 GHz range, \( N \gg 9000 \), or approximately 80 dB.

Fractional-n has been devised to allow higher \( F_r \) than the step size, yielding the slight change: \( F_0 = F_r(N + K/F) \). Higher \( F_r \) allow lowering \( N \), thus theoretically improving phase noise and allowing wider loop bandwidth and hence better switching speed.

In reality, PFD noise increases as 10log(\( F_r \)); therefore increasing \( F_r \) by 10 times improves phase noise by 10 dB (and not the theoretical 20). Even 10log(\( N \)) improvement is very significant!

However, the PFDs of fractional-n chips (so far) do not show the performance we expected, and even this gain is not realized. Many designers ask now if we really gain anything at all!

The answer is positively YES. More work is necessary to improve fractional-n PFDs and compensation performance. Advances in all-digital fractional-n should even enhance the prospects for major technological improvements in resolution, phase noise and speed. We might stand now on the brink of a “paradigm shift” in signal generation, caused by the integration of RF PLL and DSP technologies in low cost and low power chips. 1999 should be a year of breakthrough!

**PLL and fractional-n (FN) principles**

The general PLL circuit architecture is shown in Figure 1. The reference \( F_r \), \( (f_{ref}) \) is derived from a crystal and provides the “standard” from which all frequencies are derived. Long term stability and close in noise depends on crystal performance.

\[
\phi_{out} = \frac{N\phi_{ref}}{sN/F(s)K_vK_P} + \frac{N\phi_{ref}}{K_v} + \frac{1}{sN/F(s)K_vK_P} + 1
\]  \hspace{1cm} (1)

\[K = K_vK_P\]  \hspace{1cm} (2)

\[
\phi_{out} = \frac{N}{sN/F(s)K} + 1 \left( \phi_{ref} + \frac{\phi_{ref}}{K_v} \right)
\]  \hspace{1cm} (3)

\[F_0 = N \cdot F_{ref}\]  \hspace{1cm} (4)

The principle of fractional-n PLL (FN) (see Figure 3) is to use a higher reference frequency in such a way that the step size is a fractional number \( F/F_r \). Since there is no divider that divides by a fraction, FN achieves the extra resolution by instantaneously modulating the divider between \( N \) and \( N+1 \). This duty cycle, that has a value \( K/F \) (\( K \) and \( F \) are integers), determines the fractional value. Thus fractionality is achieved by averaging. An accumulator carry out drives the divider to increment by 1 each time its carry out goes to 1, as shown in Figure 3.

**Example** — In a classical PLL, for \( F_0 = 960 \) MHz and \( F_r = 30 \) kHz, \( N \) is 32000. To generate \( F_0 = 960.03 \) MHz, \( N \) will be incremented to 32001. In FN, \( F_r \) can be significantly higher than 30 kHz, say for example 16 times \( (F=16) \), so the new \( F_r \) is \( 30 \times 16 = 480 \) kHz. For \( F_0 = 960 \) MHz, the new divider \( N \) becomes 2000 (16 times less than before). To generate 960.03 MHz, the divider \( N \) will
be modulated between 2000 and 2001. For every 15 times division by 2000, there is one division by 2001. The new cycle is therefore 16 time longer than \( F_r \) (480 kHz) and generates an average frequency given by

\[ \frac{0.48(15 \times 2000 + 1 \times 2001)}{16} = 960.03 \text{ MHz}. \]

\( F_r \), the fractionality is 16 and \( K = 1 \).

When \( K = 2 \), 960.06 MHz will be generated, as shown in equation 5:

\[ F_0 = F_r(N + K/F) \] (5)

This achieves a fractional divider by a very “crude” method, because we use only the divider for the “average game.” Dividing by 1 more (from \( N \) to \( N+1 \)) means chopping the VCO phase by \( 2\pi \), so our quantizer (\( 2\pi \)) is very coarse, causing significant spurious in the signal’s spectrum. This is the equivalent, (assuming infinite loop bandwidth), to approximately \( 20 \log(\pi/\sqrt{2}) \) spurious level, convolved with the loop transfer function since the PLL is a “tracking filter.” With no filtering, (worst case) the spurious energy is +7 dBc! Figure 4 shows active and typical passive PLL network (works with charge pump detector output) and its corresponding transfer functions. These filters help create a bandpass filter transfer function that shape spectral noise and filter out spurious signals, as illustrated in Figure 2.

\[ F(s) = \frac{1+s\tau_2}{s\tau_1} \] (active filter)

\[ F(s) = (1+s\tau_1)/sC \] (7)

**Fractional mechanism (Figure 3)**

One of the more popular mechanisms used to increment the divider from \( N \) to \( N+1 \) is by asserting the carry output of an accumulator and adding its value to the counter. For example, for \( F = 16 \) use a 4 bit accumulator (which generates 16 states) when writing an input address \( K=1 \), the carry output will be 0000000000000001, for \( K=4 \) will be 0001000100010001 and so on, always generating a duty cycle of \( K/N \).

The accumulator is used mainly because of 2 reasons. First, compared to a counter, an accumulator actually generates maximum transitions. This is preferred because the spurious energy is pushed to higher frequencies where the loop can filter them out more easily.

Also, the accumulator contents represents the instantaneous phase error (always lower than \( 2\pi \)), while the carry out represents \( 2\pi \) (similar to a DDS accumulator phase weight). For example, with \( F=16 \), \( K=1 \), the accumulator output will be: 0001, 0010, 0011…1110, 1111. This (times \( 2\pi/F \)) is exactly the phase error at the sampling points. As we will see, this is used in FN circuits of the 2nd order to compensate for spurious outputs.

This method, an extension of 1st order fractional (just divider modulation), uses the accumulator contents (open loop) to compensate for the phase error. It was devised first for instruments (Racal-Dana, HP, Marconi, Fluke and others), then in PLL ASICs from Philips, Texas Instruments, National Semiconductor and Peregrine Semiconductor.

The contents of the accumulator (which exactly represents the instantaneous phase error) are used to drive a Digital to Analog converter (DAC) or another mechanism to generate analog compensation to correct the phase error. The abruptness of the phase jump, being only a multiple of \( 2\pi \) in the 1st order implementation, is transformed from a single bit quantizer to a mixed-signal multi-level quantizer with a gradual analog increment of the phase. In practice, accuracy of the analog correcting signal allows mass production with spurious suppression in the 35-40 dB range. It will be affected by temperature, aging, offsets and changes in the value of \( N \) (which affects the analog value). The loop transfer function adds attenuation and, depending on loop bandwidth, may produce spurious rejection of 65-80 dBc. This method has been coined fractional of the 2nd order.

An alternative method, 3rd order FN, now emerges, using multi-bit digital signal quantizing, coupled with oversampling and signal shaping. This allows an all digital spurious cancellation scheme with arbitrary resolution and speed, using technologies similar to those used in data conversion devices with multi level Delta Sigma modulators.
Sigma Delta modulation principles

As mentioned already, standard fractional techniques alternate the divide ratio between $N$ and $(N+1)$ in some duty cycle that produces the desired fractional value of $N+K/F$, where the division $N$ or $N+1$ at any time is an integer. The source of the spurious problem is the single bit quantization of the divide ratio and its ability to modulate the carrier only in increments of $2\pi$.

A block diagram of a Sigma-Delta modulator is shown in Figure 5. This is a single bit quantizer that generates large quantization errors which are compensated by high speed operation.

Sigma-Delta ADCs rely on oversampling the input to the point where a low resolution quantizer will produce a sufficiently accurate representation of the signal. If the input is oversampled, the dynamic range between successive samples of the signal is reduced, thus reducing the resolution requirements on the quantizer. See the Sigma-Delta modulator waveforms in Figure 7. (The corollary to FN: the sampling rate $F_r$ is much higher than the loop bandwidth).

We can further reduce the dynamic range requirements of the quantizer by considering differential quantization, where reducing the variance of the signal results in a reduction of the number of bits required in the quantizer.

Let us review shortly the principles of delta sigma data conversion; later we will use this method as an approximation of the phase compensation we need to generate, namely $2\pi K\cdot i/F$, where $i$ is the running index, time.

If an analog signal is sampled by a low resolution A/D converter, a high level of quantization error will occur. Generally, the signal to quantization error is given by:

$$\frac{S}{N_q} = 6N+1.78 \text{ dB} \quad \text{(8)}$$

This is a very well known DSP relationship. Thus, the addition of a bit in the quantizer improves $S/N_q$ by 6 dB. Assuming that the noise spectrum is flat across the clock frequency, (a reasonable approximation), this produces a flat noise density of $N_q/F_s$.

If we increase the converter clock speed, $F_s$, this noise density will decrease proportionally. However, since the signal bandwidth given by $F_b$ is fixed, the signal to noise ratio after passing the quantizer through a $F_b$ low pass filter (to regenerate the signal back) will be given by: $S/N_q(F_b/F_s)$. Now we see that while the signal to noise improves when we increase $F_s$, it improves only 3 dB, or one-half bit, per doubling $F_s$.

To summarize, oversampling helps, but not by much. If we double the frequency 10 times ($2^{10} = 1024$), and we sample a voice signal (15 kHz) by a 15 MHz signal, using a single bit quantizer will yield only signal to noise of $1 + 10.5 = 6$ bits. This is quite poor performance.

To improve on this, we can use delta sigma modulation, which shapes the noise in such a way as to “push” its energy to high frequencies, out of the $F_b$ band. The combination of oversampling and noise shaping can generate the equivalent of 1.5 bits (and more) per doubling $F_s$ frequency and more. This is very significant!

Let us analyze the transfer function of the Sigma-Delta modulator shown in Figure 7. We can simulate the
quantizer as an accurate function plus the quantization noise, which can be very large, especially if we use a single bit quantizer.

From control theory we know that the effect of any input (on the output) will be given by this input’s transfer function, given by the forward gain divided by one plus the open loop gain. Thus

\[ Y(z) = X(z) \cdot z^{-1} + (1-z^{-1}) \cdot E(z) \quad (9) \]

Where \( E(z) \) represents the contribution of the quantization error (noise), which is assumed to be uncorrelated from one sample to the next and evenly distributed over the quantization step size \( \Delta \).

Equation 9 shows that the output tracks the input with the addition of quantization noise. This noise is shaped by the 1st order differentiator (a high pass filter, \( 1 - z^{-1} \)) with a zero located at \( z = 1 \). This gives the Sigma-Delta modulator its “high pass” characteristics.

Examining noise shaping in the Fourier domain:

\[ H(\omega) = 1 - e^{-j \omega} = H(\omega) \quad (10) \]

\[ H^2(\omega) = (1 - \cos \omega t)^2 + \sin^2 \omega t \quad (11) \]

\[ H^2(\omega) = [2 \sin(\omega t/2)]^2 \quad (12) \]

For low angles, \( (F_s/F_c) \) is very low), \( H(\omega)^2 = (\omega T_s)^2 \) \( T_s \) is the sampling speed \( 1/F_s \).

Therefore, the noise is not only attenuated by \( 1/F_s \) as we showed before. Rather, the sigma delta structure adds another \( 1/F_s^2 \), together 1.5 bits per doubling \( F_c \).

Now using a single bit quantizer, multiplying \( F_s \) 10 times improves signal to quantization error to an equivalent of \( 1+10 \times 1.5 = 16 \) bits. This is the basic principle used in most CD players in the market and now will be used in PLLs as well. The block diagram of a third order sigma delta converter is shown in Figure 8.

The solution for output \( Y(z) \) for the third order system shown in Figure 8 is \( Y(z) = X(z) + E(z) \) and the general solution for an \( m \) order system is

\[ Y(z) = X(z) \cdot z^{-1} + (1-z^{-1})^m \cdot E(z) \quad (14) \]

where \( E \) is quantization noise.

Comparison

Here is a short comparative survey of integer and fractional-n PLL chips.

**Integer PLL** — There is a great variety of integer PLL parts in the market, from many sources, including National Semiconductor, Fujitsu, Philips, Texas Instruments and Plessey, to name few.

These parts are marvels of technology, being low power, low voltage, very highly integrated chips needing only 3 V, 4-6 mA. They are fully integrated and require only a VCO, crystal and loop filter. The great challenge is usually phase noise. Phase detector noise is generally given by the approximation

\[ \phi_n = L + 10 \log(F_r) \]

where \( L \) is a constant that is equivalent to the PFD noise with \( F_c = 1 \) Hz. \( \phi_n \) as function of \( F_r \) is given below for well designed PLL chips:

<table>
<thead>
<tr>
<th>( \phi_n ) (dBc/Hz)</th>
<th>( F_r ) (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>168-170</td>
<td>10 k</td>
</tr>
<tr>
<td>164-168</td>
<td>30 k</td>
</tr>
<tr>
<td>155-160</td>
<td>200 k</td>
</tr>
<tr>
<td>150-155</td>
<td>1 M</td>
</tr>
<tr>
<td>145</td>
<td>10 M</td>
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</tbody>
</table>

**Fractional-n PLL** — A good variety of fractional-n parts are already in the market from Philips, Texas Instruments and National Semiconductor. Peregrine Semiconductor will offer such chips using SOS technology in 1999.

For these parts, 2nd order fractional-n with analog compensation, a representative calculated number for PFD noise (for \( F = 8 \), and \( F_c/F_c = 30 \) kHz) is:

<table>
<thead>
<tr>
<th>( \phi_n ) (dBc/Hz)</th>
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</tr>
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<tr>
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<tr>
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As can be seen, the PFD noise level should be
improved. Performance deterioration can be caused by the additional noise from the compensation current or designs that are not mature yet. They can be improved significantly, probably by 10-15 dB, as in instrumentation, however, mass production of millions of parts is different than manufacturing instrumentation. Overall, it is quite disappointing that the main advantage of fractional at this point is the ability to improve switching speed (by opening the loop bandwidth) with no realization of phase noise advantage and operation in environments that require very high multiplications ($N$).

3rd order fractional, using delta sigma modulation —
There is always an extra level of excitement and anticipation when new technology is being introduced. There are no such chips in the market yet, not in mass production anyhow. The technology has been pioneered by Marconi UK and later at HP. Both use it successfully in instrumentation.

Synergy Microwave, in cooperation with Rohde Schwartz, has reported the development of the technology (but does not offer it as a chip yet). Philsar, a company based in Canada (www.philsar.com) has announced the development of such a chip and its availability in the market in mid-1999.

We can only anticipate the results and speculate as follows:

Using $F_r$ as reference, and a Sigma Delta modulator using 18 bit accumulators, the frequency resolution is $F_r/2^{18}$, which calculates to 40 Hz with 10 MHz reference.

There should be no spurious in the signal’s spectrum. With a loop bandwidth of 50 kHz (50 k/10 M = .005), switching speed will be in the order of 30-40 µsec. The division ratio for cellular is 100 and for PCS it is on the order of 180. Therefore, noise penalty (20log$N$) will be low, and estimated phase noise profile could be as good as shown in Figure 9.

Of course there is a lot of work to do, but we are anticipating 3 V operation, all functions on one or two chips, with low current (<20 mA).

**Conclusion**

PLL technology is evolving in two directions. One is mainly in IC technology, reducing geometries, allowing better integration, functionality, voltage and power. The other is the integration of PLL with DSP and, resulting in advanced fractional-N solution that allow better phase noise performance and improved switching speed. Fractional-N technology currently has a very modest presence in the PLL universe, but this will change in the near future. FN requires only modest increase in complexity and therefore allow significant improvement at very marginal increase in cost.

All-digital fractional-n still requires theoretical work and ASIC development to achieve the level of maturity needed for manufacturing. We expect this to happen within the next 3-5 years. Additional focus will be on switching speed as fast hopping becomes a networking and diversity technology. Of course, lowering operating voltage and current will get attention, as well.

RF engineering now requires good basic knowledge of DSP. These RF/DSP synthesizers are exciting and interesting challenges for design engineers, reaching another level of evolution in wireless communications.

**References**


**Author information**

Bar-Giora Goldberg was co-founder and chief technical officer of Sciteq Electronics, where he spent 15 years developing PLL and DDS technology and products. He has authored 6 U.S. patents, the book *Digital Techniques in Frequency Synthesis*, and numerous articles. He is also cooperating with Besser Associates, giving seminars in the U.S. and abroad on Frequency Synthesis and Communication Theory. Residing in San Diego, he has recently founded Vitacomm, a company dedicated to signal generation and timing technology for wireless and networking. He can be reached by Email at giora18@tns.net, by telephone at 619-846-1071 or by fax at 619-452-6649.

First attempt to write a comprehensive text on the subject of digital frequency synthesis, direct digital synthesis, and digital and fractional-N synthesis; and the number of sources is not overwhelming in this newly emerging technological discipline. We have found a paucity of literature in the field; and even though many articles have begun to appear in the last few years and the technology attracts much attention in professional meetings, comprehensive texts and bibliographies are needed. This is what this text attempts to supply. Every attempt is made to present a very comprehensive, up...


Fractional phase-locked loops (fPLLs) offer all the features available in previous-generation Altera® PLLs. You can find fPLLs in Altera’s 28-nm devices, including Stratix® V, Arria® V, and Cyclone® V FPGAs. New capabilities are shown in Table 1. Table 1: New Capabilities Provided by fPLLs. Feature Description. fPLLs in 28-nm FPGAs. Replacement of reference clock oscillators. Transceiver transmit PLL. Precision Fractional Frequency Synthesis. A major innovation in our 28-nm devices is the integration of fPLLs into the device architecture. All general-purpose PLLs are implemented as fPLLs, capable of advanced fractional frequency synthesis, as well as standard M/N multiplication. Depending on device density, up to 32 fPLLs are available for general-purpose use. Fractional-N Frequency Synthesizers. Going Digital "Outline of PLL Short Course. Popular VCO Structures." Summary of Fractional-N Frequency Synthesizers. Short Course On Phase-Locked Loops IEEE Circuit and System Society, San Diego, CA. Analog Frequency Synthesizers. Michael H. Perrott September 16, 2009. Copyright © 2009 by Michael H. Perrott All rights reserved. AN-1879 Fractional N Frequency Synthesis. Submit Documentation Feedback. Copyright © 2008â€“2013, Texas Instruments Incorporated. The phase detector frequency increases. For this situation, the phase noise is proportional to 10·log (NNew / NOld). In other words, if the N counter value is decreased by a factor of 10 with the output frequency held constant, then the phase detector frequency will increase by a factor of 10 and the PLL flat noise will improve by 10 dB. However, this phase noise improvement may be masked at some offsets by the 1/f. The avid reader, the AN-1865 Frequency Synthesis and Planning for PLL Architectures Application Report. (SNA061) goes into more detail of how to calculate the GCD and calculate frequencies for fractional PLLs.